AF

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/751,813
Filing Date	December 29, 2000
First Named Inventor	Brinkley Sprunt
Art Unit	2192
Examiner Name	Yigdall, Michael J.
Total Number of Pages in This Submission	25
Attorney Docket Number	42390P8258

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
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  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
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- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Signature	Ashley Ott
Date	August 18, 2006

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Typed or printed name	**Pat Sullivan**		
Signature	Pat Sullivan	Date	**August 18, 2006**

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	09/751,813
Filing Date	December 29, 2000
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METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
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				SUBTOTAL (2)	($) 500.00

SUBMITTED BY Complete (if applicable)

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Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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Our Docket No.: 042390.P8258

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sprunt	)	Examiner: Yigdall, Michael J.
Application No.: 09/751,813	)	**Art Group: 2192**
Filed: December 29, 2000	)	
For: Qualification of Event Detection by Thread ID and Thread Privilege Level	)	

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereinafter "Appellant") hereby submits this Brief in support of its appeal from a final decision by the Examiner, mailed March 17, 2006, in the above-referenced Application. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences (hereinafter "Board") for allowance of the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 are currently pending in the above-referenced application. In the Final Office Action mailed March 17, 2006 (hereinafter "Final Office Action"), claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Larsen et al. (U.S. Patent No. 5,835,705) ("*Larsen*") in view of Diepstraten et al. (U.S. Patent No. 6,205,468) ("*Diepstraten*") and further in view of Dreyer et al. (U.S. Patent No. 5,657,253 ("*Dreyer*").

IV. STATUS OF AMENDMENTS

Claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 are currently pending in the above-referenced application. These claims were finally rejected in the Final Office Action. The Examiner confirmed the final rejection of these claims in an Advisory Action mailed June 7, 2006 (hereinafter "Advisory Action").

In response to the Final Office Action, rejecting claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 under 35 U.S.C. §103(a), Appellant filed a Response After Final pursuant to 37 C.F.R. § 1.116 on May 11, 2006. Amendments to claims 1 and 18 were made to correct matters of form. Subsequently, the Advisory Action maintaining all rejections in the Final Office Action was mailed. The Advisory Action entered the amendments made in the Response After Final. In response to the Advisory Action, Appellant filed a Notice of Appeal on June 19, 2006. A copy of all claims on appeal is attached hereto as an Appendix of Claims.

Appellant respectfully traverses each of these grounds of rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

According to one embodiment, an apparatus of claim 1 is described. The apparatus includes a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event. (Figure 1, ref. 10; Specification at pg. 9.) The apparatus also includes an event selection control register (ESCR) coupled to the processor. (Figure 1, ref. 30; Spec. at pgs. 9-11.) Furthermore, the apparatus includes a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor. (Figure 1, ref. 40; Spec. at pg. 11.) Additionally, the apparatus includes a second

multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. (Figure 1, ref. 50; Spec. at pg. 11.) The apparatus also includes a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred. (Figure 1, ref. 60; Spec. at pgs. 13-14.) Finally, the apparatus includes an event counter to count the event qualified by the logic circuit. (Figure 1, ref. 70; Spec. at pg. 14.)

In another embodiment, a method of independent claim 18 discloses the operation of executing a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event. (Specification at pg. 9.) Then, the method discloses instructing a first multiplexer, based on a first set of signals from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor. (Id. at pg. 11.) Subsequently, the method discloses instructing a second multiplexer, based on a second set of signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. (Id. at pg. 11.) Then, the method discloses qualifying the event, by a logic circuit, based on a thread ID and a thread CPL, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred. (Id. at pgs. 12-14.) Next, the method discloses counting the event qualified by the logic circuit using an event counter. (Id. at pg. 14.) Finally, the method discloses accessing the event counter to determine a current count of the event. (Id. at pg. 15.)

In yet a further embodiment, a system of independent claim 32 is disclosed. The system includes a storage medium coupled with a processor, the processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event. (Figure 1, ref. 10; Spec. at pg. 9.) The system also includes an event selection control register (ESCR) coupled to the processor. (Figure 1, ref. 30; Spec. at pgs. 9-11.) The system further includes a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor. (Figure 1, ref. 40; Spec. at pg. 11.) In addition, the system includes a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. (Figure 1, ref. 50; Spec. at pg. 11.) The system includes a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred. (Figure 1, ref. 60; Spec. at pgs. 13-14.) Furthermore, the system includes an event counter to count the event qualified by the logic circuit. (Figure 1, ref. 70; Spec. at pg. 14.) Finally, the system includes an access location to allow access to the event counter to determine a current count of the event. (Spec. at pgs. 14-15.)

Finally, a machine-readable medium of independent claim 40 is disclosed. The machine-readable medium includes data representing sets of instructions, the sets of instructions which, when executed by a machine, cause the machine to: execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (specification at pg. 9); instruct a first multiplexer, based on a first set of signals

from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor (id. at pg. 11); instruct a second multiplexer, based on a second set of control signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked (id. at pg. 11); qualify the event, by a logic circuit, based on a thread ID and a thread CPL, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (id. at pgs. 12-14); count the event qualified by the logic circuit using an event counter (id. at pg. 14); and access the event counter to determine a current count of the event (id. at pg. 15).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Larsen et al. (U.S. Patent No. 5,835,705) ("*Larsen*") in view of Diepstraten et al. (U.S. Patent No. 6,205,468) ("*Diepstraten*") and further in view of Dreyer et al. (U.S. Patent No. 5,657,253 ("*Dreyer*").

VII. ARGUMENT

A. THE PENDING CLAIMS 1, 3, 4, 7-9, 18, 20, 21, and 27-45 WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE ANY COMBINATION OF THE PRIOR ART REFERENCES *LARSEN, DIEPSTRATEN,* AND *DREYER* DOES NOT DISCLOSE OR SUGGEST EACH AND EVERY FEATURE OF THE PENDING CLAIMS

Appellant respectfully submits that *Larsen* in view of *Diepstraten* and further in view of *Dreyer* fails to disclose or suggest the claimed invention for the reasons set forth below. As the Honorable Board is well aware, in order to establish a *prima facie* case of obviousness:

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, Revision 2, May 2004, §2143.

(1) Claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 were improperly rejected because *Larsen* in view of *Diepstraten* and further in view of *Dreyer* does not disclose or suggest a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of a class of events in order to select an event that belongs to a subclass that is not masked

Claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 each recite an element that is not disclosed by the combination of *Larsen*, *Diepstraten*, and *Dreyer*. For example, Appellant's independent claim 1 recites the following:

An apparatus, comprising:

a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

an event selection control register (ESCR) coupled to the processor;

a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor;

a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred; and

an event counter to count the event qualified by the logic circuit.

Appellant's independent claims 18, 32, and 40 recite similar features to those of independent claim 1.

Larsen discloses a system for performance monitoring within a multithreaded processor. (*Larsen* at Abstract.) *Larsen* discloses that "the processor has first and second modes of operation... [and] when the performance monitor is operating in the first mode, a first counter within the performance monitor increments in response to each occurrence of the first event and a second counter within the performance monitor increments in response to each occurrence of the second event" (Id. at col. 2, lines 2-9.) *Larsen* additionally discloses using a performance monitor to receive as inputs selected event occurrences. These event occurrences are recorded by Performance Monitor Counters (PMCs) within the performance monitor and the performance monitor outputs the value of specified PMCs. (Id. at col. 4, lines 46-64.) *Larsen* further discloses "in global mode the event occurrences generated by all of the logical partitions of processor are input into multiplexer. Multiplexer then routes the event occurrences to particular counters among PMCs in response to select input." (Id. at col. 5, lines 7-11).

Diepstraten discloses a context controller for managing multitasking in a processor. (*Diepstraten* at Abstract.) The context controller includes: (1) an event recorder that records occurrences of events, and (2) an encoder, associated with the event recorder, that, in response to a software instruction, priority encodes bits corresponding to at least some of the events to generate an event-dependent vector to allow the processor to branch as a function thereof. (Id. at col. 4, ll. 2-8.) "Context", for the purposes of *Diepstraten*, is defined as all processor state information that would be of use in restoring the processor to a given state. (Id. at ll. 19-22.) In one embodiment of *Diepstraten*, the context controller further includes an event masker, associated with the event recorder and the encoder, which masks ones of the events to yield at least some of the events. (Id. at ll. 41-44.)

Dreyer discloses an apparatus for measuring and monitoring various parameters that contribute to the performance of a processor. (*Dreyer* at Abstract.) The apparatus includes a plurality of programmable event counters for counting a number of independent events selected from a predetermined list of processor events which normally occur during the operation of the processor. (Id. at col. 1, ll. 54-58.) A specialized register in *Dreyer* controls the operation of the event counters and also selects the events to be counted. (Id. at ll. 59-61.) The contents of the event counters can be accessed either by a supervisor mode program which reads an instruction or through a special access port. (Id. at col. 1, ln. 66-col. 2, ln. 3.)

Appellant submits that *Larsen* does not disclose or suggest a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of a class of events in order to select an event that belongs to a subclass that is not masked. The Final Office Action acknowledges as much by stating "*Larsen* does not expressly disclose: (d) a second multiplexer coupled to the

ECSR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked." (Final Office Action at pg. 4.) However, the Final Office Action does rely on *Diepstraten* as disclosing this feature. (Id.)

Appellant further submits that *Diepstraten* does not disclose or suggest such a feature. The Final Office Action cites *Diepstraten* at column 4, lines 42-50 and the event mask register 90 of Figure 3 as disclosing this feature. However, appellant submits that neither of these cited portions of *Diepstraten* disclose or suggest a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

With reference to column 4, lines 42-47 of *Diepstraten*, this cited portion states:

> [T]he context controller further includes an event masker, associated with the event recorder and the encoder, that masks ones of the events to yield the at least some of the events. Event masking may therefore optionally be employed to reduce the number of events factored into encoding and vector generation.

Nowhere in this cited portion is there disclosed ***a second multiplexer coupled to a first multiplexer and an ESCR to mask, based on control signals from the ESCR, subclasses of a class of events selected by the first multiplexer to result in an event that is not masked***. Although *Diepstraten* may be generally discussing event masking in this context, it does not disclose the structure provided by the cited feature of claim 1. Namely, it does not disclose the connections of the second multiplexer to a first multiplexer and an ESCR. Nor does this relied-upon portion of *Diepstraten* disclose the functioning of the second multiplexer, where it masks a class of events received from the first multiplexer based on control signals from an ESCR.

The Final Office Action additionally points to the event mask register 90 of Figure 3 (or "event masker") of *Diepstraten* as disclosing the above-cited feature of claim 1. (Final Office Action at pg. 4.) First, the description in *Diepstraten* of the structure and functioning of the event mask register 90 at column 12, lines 36-57 does not disclose the structure and functioning of the second multiplexer, as provided in the cited feature of claim 1.

The structure of the event mask register 90 of *Diepstraten* is not the same as the structure of the second multiplexer because the event mask register is not connected to a first multiplexer and also to an ESCR. The Advisory Action states that "[t]he event mask register 90 is the event masker's control register (see, for example, column 12, lines 36-57)" in order to provide disclosure support for the connection between the second multiplexer and the ESCR as provided in claim 1. (Advisory Action at continuation sheet.) However, appellant can find no disclosure or suggestion in *Diepstraten* of a separate "event masker" unit controlled by the event mask register 90. The only discussion of an "event masker" in *Diepstraten* is at column 4, lines 42-47. Yet, nothing in this cited portion suggests that the "event masker" is controlled by event mask register 90. Rather, appellant submits that the event mask register 90 is the "event masker" referred to in this portion. As such, the structure of the event mask register 90 (or event masker) of *Diepstraten* is not the same as the structure of the second multiplexer because there is no disclosure or suggestion of a connection to a first multiplexer and an ESCR in *Diepstraten*.

Furthermore, the functioning of the event mask register 90 of *Diepstraten* is the not the same as the functioning of the second multiplexer because it does not mask a class of events received from the first multiplexer based on control signals from the ESCR. (See, e.g., *Diepstraten* at col. 12, ll. 36-57.) The Advisory Action states that *Diepstraten*

discloses that the event masker "masks ones of the events to yield at least some of the events." (Advisory Action at continuation sheet.) Yet, there is no disclosure or suggestion of the event masker (i.e., event mask register 90) being masking event based on control signals from an ESCR. As such, the functioning of the event masker (event mask register 90) is not the same as the functioning of the second multiplexer which masks subclasses of event based on control signals from the ESCR.

Second, this event mask register is not a multiplexer at all; rather, it is a register. The Final Office Action explains around this difference by stating that "[a]lthough *Diepstraten* does not expressly disclose that the event masker is a multiplexer, *Larsen* already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36)." (Final Office Action. at pg. 5.) However, the two multiplexers illustrated in Figure 3 of *Larsen* and described at column 5, lines 30-36 of *Larsen* only ***operate concurrently, or in parallel,*** on separate different threads in a multithreaded processor. (*Larsen* at Fig. 3 & col. 5, ll. 22-36.) They do not operate as provided by the cited feature of claim 1 by having the first multiplexer select a class of events, and then further having the second multiplexer mask this resulting class of events according to subclasses to select an event. Appellant can find no disclosure or suggestion in Larsen of such dependency between the multiplexers of *Larsen*. Therefore, *Larsen* does not actually "suggest implementing such event selection as multiplexers".

Finally, appellant submits that *Dreyer* does not disclose or suggest the cited feature of claim 1. The Final Office Action does not rely on *Dreyer* as disclosing this feature, nor can appellant find any disclosure or suggestion of this feature anywhere in *Dreyer*.

Therefore, as none of *Larsen*, *Diepstraten*, or *Dreyer* individually disclose or suggest a second multiplexer coupled to the ESCR and the first multiplexer to mask, based

on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked, any combination of *Larsen*, *Diepstraten*, and *Dreyer* does not disclose or suggest this feature. The Advisory Action states that the above statement is not persuasive against an obviousness rejection because "[o]ne cannot show nonobviousness by attacking references individually where the rejections are based on combination of references". (Advisory Action at continuation sheet.) The Advisory Action continues by stating that "the test for nonobviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art." (Id.) However, it is still a requirement to establish an obviousness rejection that the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***." (*In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP at §2143; emphasis added.)

Accordingly, if none of the prior art references *Larsen*, *Diepstraten*, and *Dreyer* discloses a particular feature of a claim, then logically there is no possibility that the combination of the references can disclose or suggest the feature. Appellant has merely argued that ***none*** of the provided references disclose or suggest a particular feature of a claim, and as a result, the combined teaching of these references cannot disclose or suggest this feature. As appellant has shown above, none of *Larsen*, *Diepstraten*, or *Dreyer* disclose a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. Therefore, independent claim 1 is patentable over the combination of *Larsen*, *Diepstraten*, and *Dreyer*.

Therefore, as none of *Larsen*, *Diepstraten*, or *Dreyer* individually disclose or suggest a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on

a second set of control signals from the ESCR, subclasses of a class of events in order to select an event that belongs to a subclass that is not masked, Appellant submits that any combination of *Larsen*, *Diepstraten*, and *Dreyer* also does not disclose or suggest such a feature. Therefore, independent claims 1, 18, 32, and 40 are patentable over *Larsen* in view of *Diepstraten* and further in view of *Dreyer*.

Claims 3, 4, 7-9, 20, 21, 27-31, 33-39, and 41-45 variously depend from claims 1, 18, 32, and 40. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that claims 3, 4, 7-9, 20, 21, 27-31, 33-39, and 41-45 are similarly patentable over *Larsen* in view of *Diepstraten* and further in view of *Dreyer*.

For the foregoing reasons, Appellant submits that the Examiner has failed to search and find a printed publication or patent that discloses the claimed invention as set forth in MPEP § 706.02(a). Thus, the Examiner erred in rejecting claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 under U.S.C. § 103(a).

VIII. CONCLUSION

Careful review of the Examiner's rejections shows that the Examiner has failed to provide any reference, or combination of references of the prior art that shows all of the elements of each appealed claim. Therefore, Appellant respectfully submits that all appealed claims in this application are patentable and were improperly rejected by the Examiner during prosecution before the United States Patent and Trademark Office. Appellant respectfully requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted with a check for $500.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: August 18, 2006

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IX. APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(1)(viii))

The claims on appeal read as follows:

1. An apparatus, comprising:

a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

an event selection control register (ESCR) coupled to the processor;

a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor;

a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred; and

an event counter to count the event qualified by the logic circuit.

2. (Cancelled)

3. The apparatus of claim 1, wherein the ESCR comprises a first field of bits to store the first set of control signals to select the class of events.

4. The apparatus of claim 3, wherein the ESCR further comprises a second field of bits to store the second set of control signals to mask the subclasses.

5-6. (Cancelled)

7. The apparatus of claim 1, wherein the event counter is stopped and cleared before a new event is selected.

8. The apparatus of claim 7, wherein the event counter is preset to a certain state.

9. The apparatus of claim 1, wherein the class of events includes hardware performance and breakpoint events.

10-17. (Cancelled)

18. A method, comprising:

executing a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

instructing a first multiplexer, based on a first set of signals from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor;

instructing a second multiplexer, based on a second set of signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

qualifying the event, by a logic circuit, based on a thread ID and a thread CPL, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred;

counting the event qualified by the logic circuit using an event counter; and

accessing the event counter to determine a current count of the event.

19. (Cancelled)

20. The method in claim 18, wherein the qualifying the event includes requiring that the event has a preselected thread ID.

21. The method in claim 20, wherein the qualifying the event further includes requiring that the event has a preselected thread CPL.

22-26. (Cancelled)

27. The method of claim 18, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

28. The method of claim 20, wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred.

29. The method of claim 21, wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred.

30. The apparatus of claim 1, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

31. The apparatus of claim 1, further comprising an access location to allow access to the event counter to determine a current count of the event.

32. A system, comprising:

a storage medium coupled with a processor, the processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

an event selection control register (ESCR) coupled to the processor; a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor;

a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred;

an event counter to count the event qualified by the logic circuit; and

an access location to allow access to the event counter to determine a current count of the event.

33. The system of claim 32, wherein the access location allows access to determine the count without disturbing the operation of event counter.

34. The system of claim 33, wherein the ESCR comprises a first field of bits to store the first set of control signals to select the class of events.

35. The system of claim 34, wherein the ESCR further comprises a second field of bits to store the second set of control signals to mask the subclasses.

36. The system of claim 32, wherein the event counter is stopped and cleared before a new event is selected.

37. The system of claim 36, wherein the event counter is preset to a certain state.

38. The system of claim 32, wherein the class of events includes hardware performance and breakpoint events.

39. The system of claim 32, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

40. A machine-readable medium having stored thereon data representing sets of instructions, the sets of instructions which, when executed by a machine, cause the machine to:

execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

instruct a first multiplexer, based on a first set of signals from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor;

instruct a second multiplexer, based on a second set of control signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

qualify the event, by a logic circuit, based on a thread ID and a thread CPL, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred;

count the event qualified by the logic circuit using an event counter; and

access the event counter to determine a current count of the event.

41. The machine-readable medium of claim 40, wherein to qualify the event includes requiring that the event has a preselected thread ID.

42. The machine-readable medium in claim 41, wherein to qualify the event further includes requiring that the event has a preselected thread CPL.

43. The machine-readable medium of claim 40, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

44. The machine-readable medium of claim 40, wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred.

45. The machine-readable medium of claim 41, wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred.